SYNOPSYS®

Shift Left to Accelerate Your Vehicle Design Process

A Primer on Our Triple Shift Left Methodology

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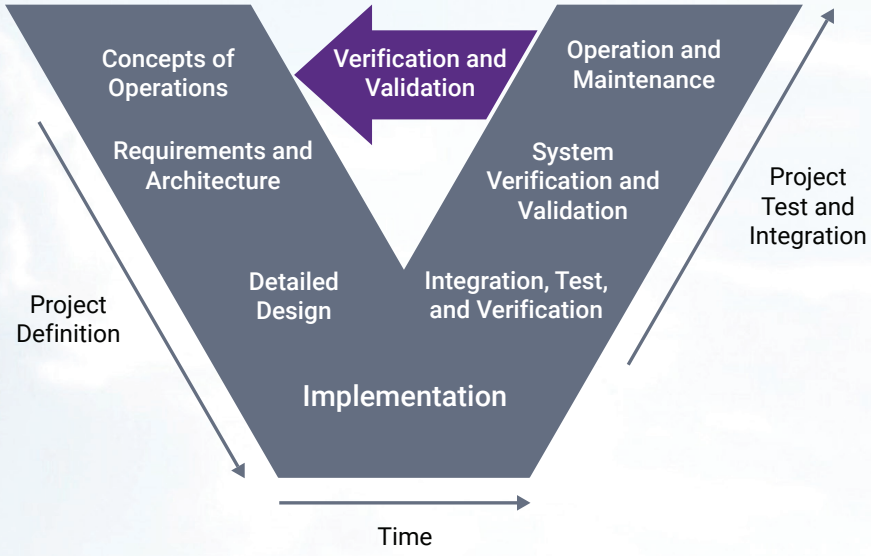
Powering Automotive Innovation—from System to Software and Silicon

What does it mean to shift left when it comes to automotive design? It's about finding the best solution to your problem and ensuring its feasibility during design as early as possible—well before testing. And delivering safety, security, reliability, and quality across the automotive digital value chain.

Big data and automated capabilities are helping to make cars safer, but they're also presenting a major disruption in the automotive development process. What's more, the constant evolution of automotive architectures, as well as the need for the highest levels of optimized computing power for applications like in-vehicle entertainment and autonomous driving, demand highly integrated, optimized SoCs.

The Synopsys Triple Shift Left methodology presents a way forward by transforming a traditionally serial automotive development process into a parallel one.

The idea of shifting left comes from the software industry and its drive to improve and optimize prior to testing. Rather than a linear flow, the Synopsys methodology is based on the V-model and agile development process, where each phase of the development lifecycle is tied to its associated testing phase/sprints. The idea is to provide greater flexibility and agility into the cycle, while identifying opportunities for enhancement early on.



Given the high stakes of the semiconductor world, a shift-left approach equips you to address the unique challenges of the automotive industry. Our Triple Shift Left methodology covers three key areas:

- Shift #1 covers the system level, helping you—based on your functional requirements—to explore electrical/electronic (E/E) architectural design options, optimize and validate your electronic component choices, and evaluate tradeoffs to avoid unexpected hardware resource bottlenecks. We will support you in optimizing your architecture, balancing it for performance and cost and with automotive-grade solutions.
- Shift #2 is all about software development, with a focus on helping you significantly accelerate development cycle times and testing through virtualized SoCs and electronic control units (ECUs) well before hardware availability. All this without compromising on functional safety and security, while targeting zero defects.
- Shift #3 centers on the silicon, helping you accelerate the development of robust, safe, and secure automotive-compliant SoCs through automotive-grade building blocks, design and verification flows, and expert services around safety, security, reliability, and quality. As a result, we can support you in reaching your target BOM value.

What's the "Triple" in Triple Shift Left?

Today's advanced vehicles commonly contain far more than 100 million lines of code and beyond 100 ECUs to run various functions. For all of these components, Triple Shift Left helps you meet time-to-market goals as well as hit your product integrity targets: safety, security, reliability, and quality.

From safety-critical advanced driver assistance systems (ADAS) and highly automated driving (AD) to engaging infotainment consoles, the automotive features available rely on advanced technologies that must work as intended. Triple Shift Left applies to all innovation areas in automotive, including electric vehicle (EV) powertrain control functions, new zonal architectures, in-vehicle information and entertainment systems, and high-performance compute autonomous drive systems.

Let's take a closer look at each shift.

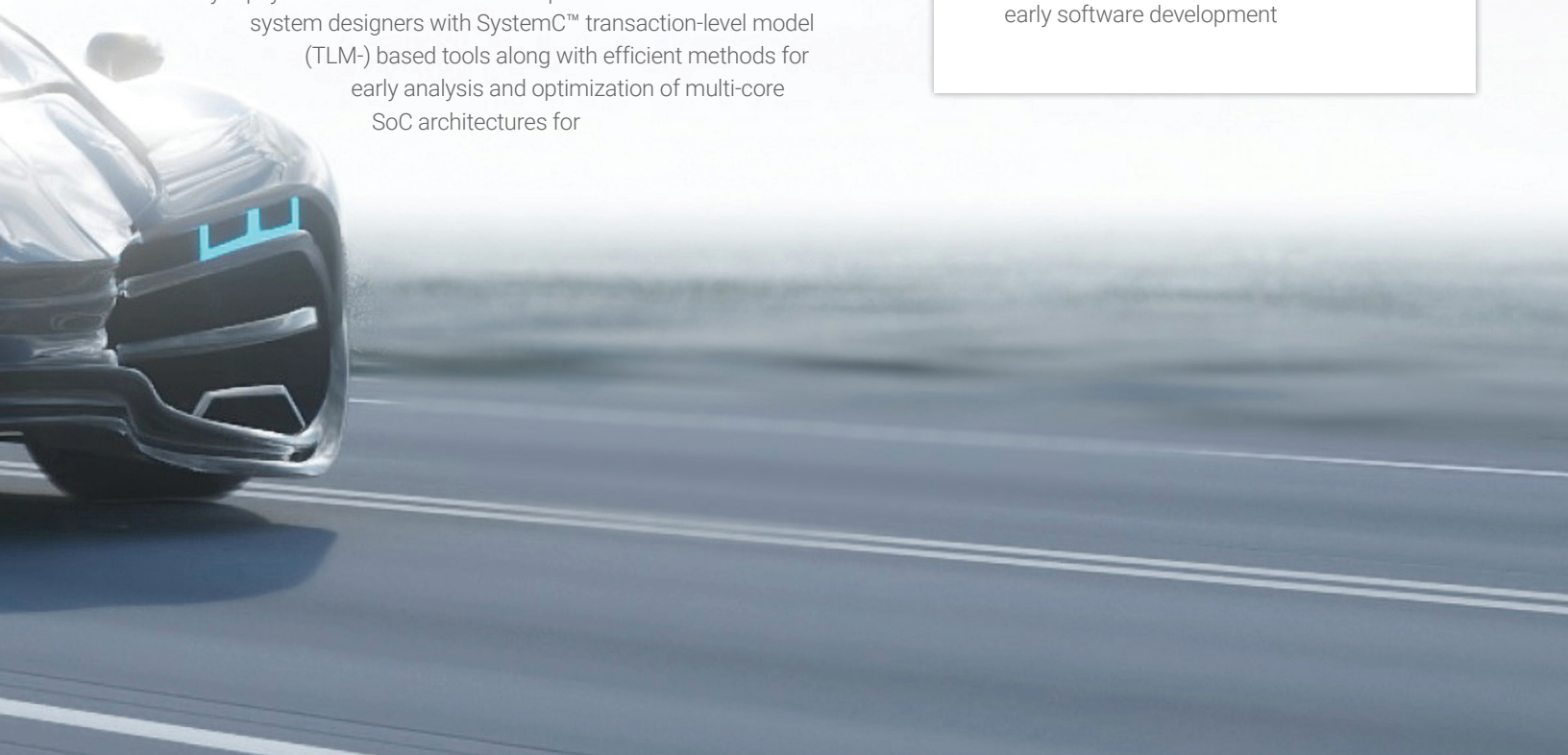
Shift #1: Avoiding Bottlenecks at the System Level

Shift #1 addresses **system development**, focusing on early dynamic analysis and optimization of architectures with multiple ECUs, including mechatronics. An architectural model allows fast, dynamic simulations to find performance, traffic, latency, and power bottlenecks in the system—before you start to realize hardware.

Tools that play a central role in this phase include those that provide early analysis and optimization of multi-core SoC architectures, along with early software development kits and virtual prototyping solutions. For example, Synopsys Platform Architect™ Ultra provides architects and system designers with SystemC™ transaction-level model (TLM-) based tools along with efficient methods for early analysis and optimization of multi-core SoC architectures for

Shift #1 Solutions

- Synopsys Platform Architect Ultra for early analysis and optimization of multi-core SoC architectures
- SaberRD® robust design methods for mixed-signal, mixed-domain power electronic and mechatronic systems
- Virtualizer Development Kits (VDKs) for early software development



performance and power. The Virtualizer™ solution uses advanced modeling tools for accelerated development and deployment of virtual prototypes. Complementing this is the Saber platform for automotive, which lets you design and verify the interaction of multiple technologies (electrical, mechanical, hydraulic, magnetic, software, etc.). With Saber, you can create virtual prototypes of your system, including the wire harness, to reduce the number of design iterations and hardware prototypes.

Our Shift #1 approach for system development guides you to meet your design performance requirements while achieving tight time-to-market targets.

Shift #2: Starting Software Development Earlier

Shift #2 is about **software development**, with an emphasis on early development of safe and secure software and testing it on virtualized hardware and operating systems. This phase is about increasing coverage, accelerating test cycles, and using automated regression to allow frequent software updates.

Shift #2 Solutions

- Virtualizer virtual prototyping development environment
- VDKs for early software development
- QTronic virtual ECU for fast feedback on automotive application software
- HAPS® FPGA-based prototyping
- Hybrid prototyping
- Virtual prototyping services
- Defensics fuzz testing platform
- Coverity® static application security testing
- Black Duck Open Source management
- CodeDx platform for automating key workflows to enhance speed and security

Through our virtual prototyping solutions and VDKs, Synopsys provides early access to silicon chips and virtual ECUs, so software development can start up to 18 months earlier, well before hardware becomes available. With our virtual models, Synopsys helps you create test platforms for virtual vehicle development. Then, you'll be prepared to engage in extensive verification through static security testing, software composition analysis, interactive security testing, and fuzz testing.

Even after hardware is available, virtualized ECUs boost software integration and regression testing across distributed software development teams. This approach is much more scalable and cost effective than shipping around development boards. In parallel, our software integrity solutions enable you to ensure the highest levels of software safety, security, reliability, and quality through rigorous testing and validation.

With our Shift #2 approach for software development, you can get a head start on building security and quality into all stages of your automotive software lifecycle.

Shift #3: Faster SoC Design and Verification

Shift #3 centers on **SoC development**, prescribing accelerated development of robust, safe, and secure automotive-compliant SoCs with automotive-grade building blocks and design flows. Using pre-designed, pre-verified IP to implement dedicated functions on silicon saves time and effort versus developing these functions from scratch. Tools certified to automotive standards along with flows designed to support product safety compliance help you deliver a safe, secure, and reliable ride.

To support this shift, Synopsys provides IP and design flows, as well as expert services. We accelerate automotive SoC design and qualification by delivering the broadest portfolio of automotive-grade DesignWare® Interface, Processor, Security, and Foundation IP with the highest levels of safety, security, reliability, and quality. Our hardware/software co-design and Verification Continuum® solutions allow you to connect the entire automotive value chain during the SoC development process and avoid unnecessary iterations.

Shift #3 Solutions

- DesignWare IP for automotive
- HAPS FPGA-based prototyping
- Hybrid prototyping
- Hybrid emulation
- Verification Continuum
- Safety-aware solutions

Our comprehensive, safety-aware solution automates design and verification of functional safety measures to make SoC design highly predictable and reach the target Automotive Safety Integrity Level (ASIL), a key element of the ISO 26262 automotive functional safety standard. And, with our emulation and FPGA prototyping solutions along with the virtual platforms highlighted in Shift #2, you'll be well equipped to accelerate your overall design and verification process with our Shift #3 for SoC development.

What does the future of automotive design look like? Tomorrow's cars will depend even more on efficient silicon chips, integrating more capabilities while reliably processing massive amounts of code and data. Our Triple Shift Left methodology gives you the tools to implement your functional requirements as well as cost and performance targets efficiently into an automotive-grade SoC design. With this approach, you'll be well on the road to innovating from system to software and silicon to create robust architectures with headroom for the future.

Why Choose Synopsys?

Broad portfolio of automotive products across design, verification, IP, and security segments, making Synopsys your single-source development partner from E/E system architecture to SoC design

Automotive product breadth and maturity: safety, security, reliability, and quality across the automotive digital value chain, with solutions certified to ISO 26262 and AEC-Q100

Automotive experience: 14 of Top 15 automotive OEMs use our software security solutions

Global availability: international footprint, with a presence in 30+ countries

Established leader in the complete value chain, from system to low-level chip design; No. 1 in interface, analog, embedded memories, and physical IP

SYNOPSYS®
Silicon to Software™

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